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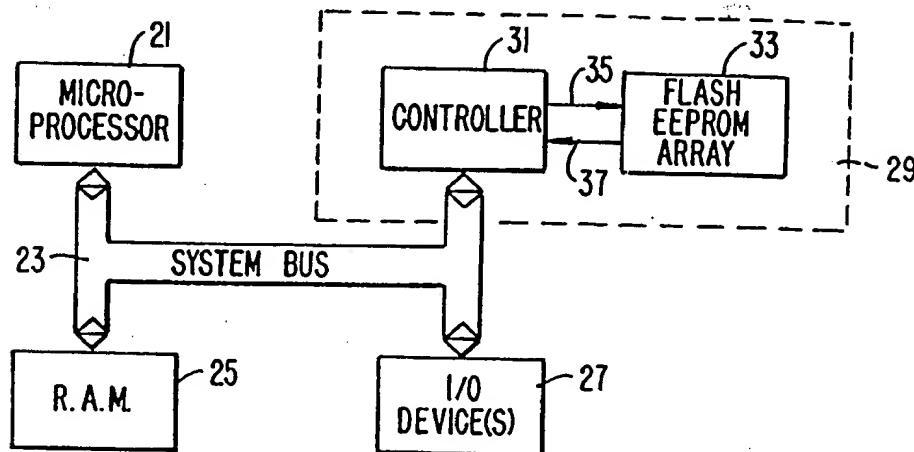


FIG._1A

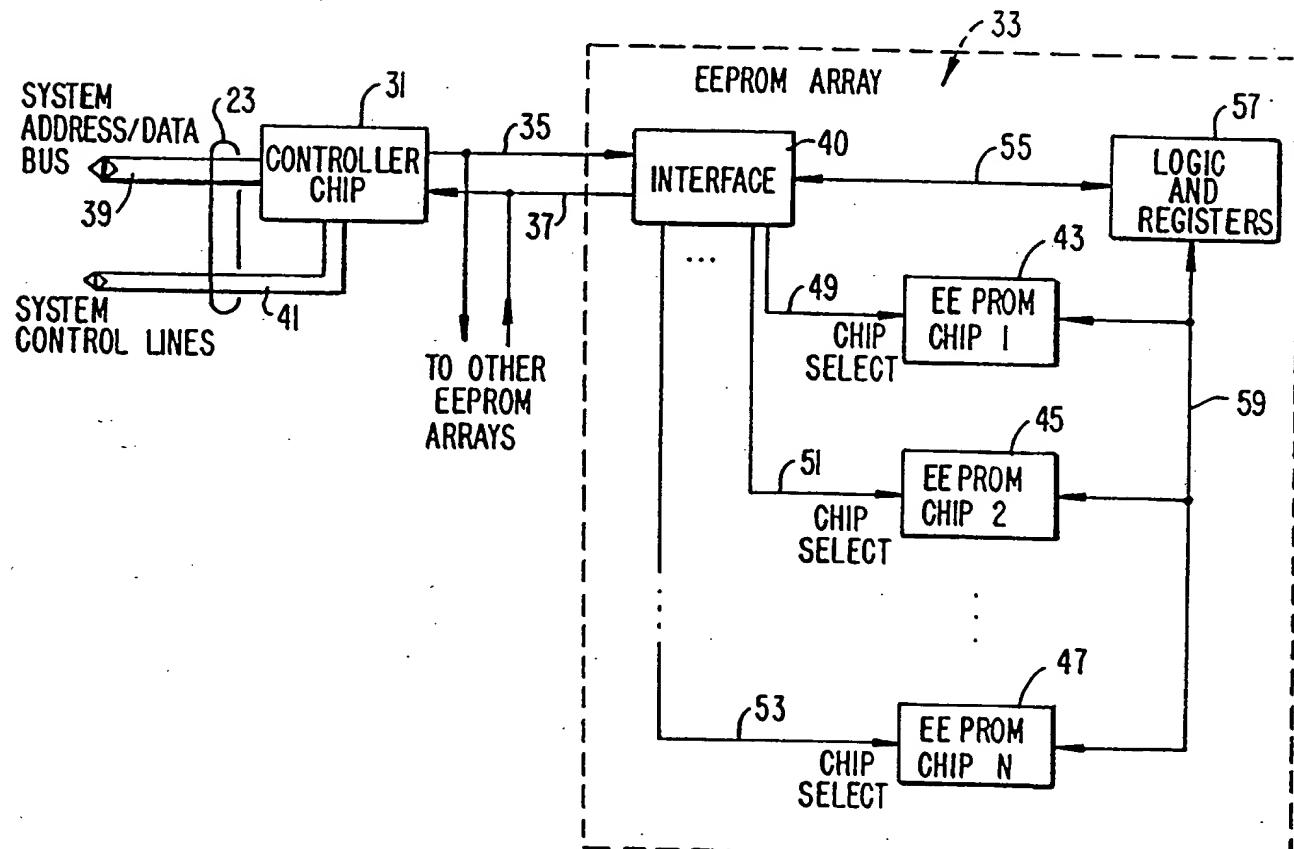


FIG._1B



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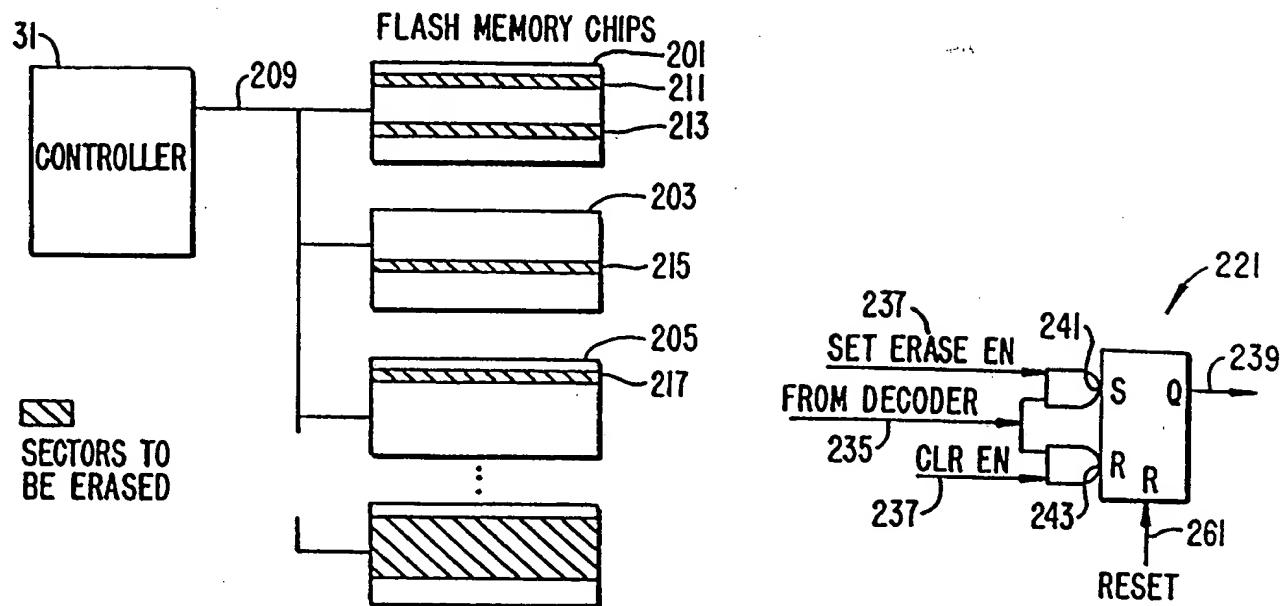


FIG. 2

FIG. 3B

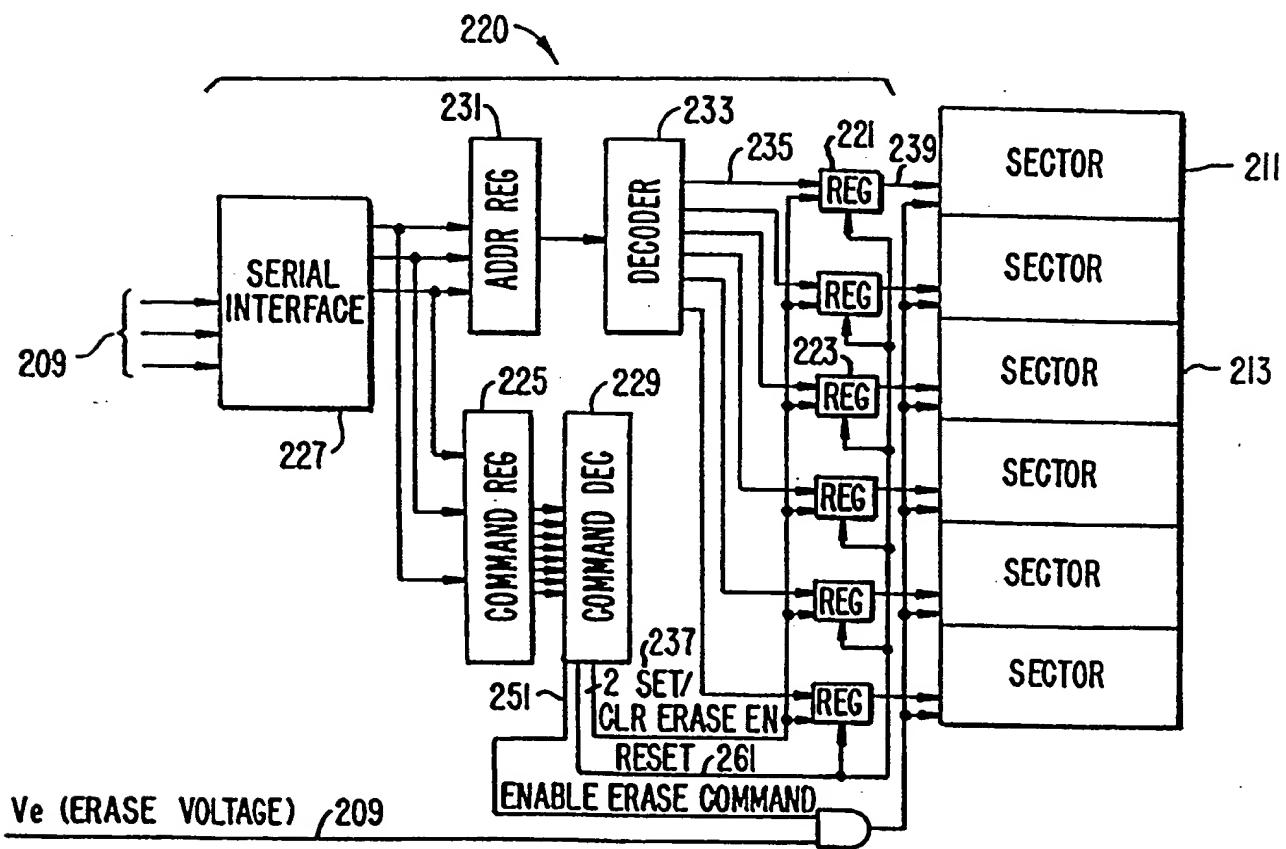


FIG. 3A



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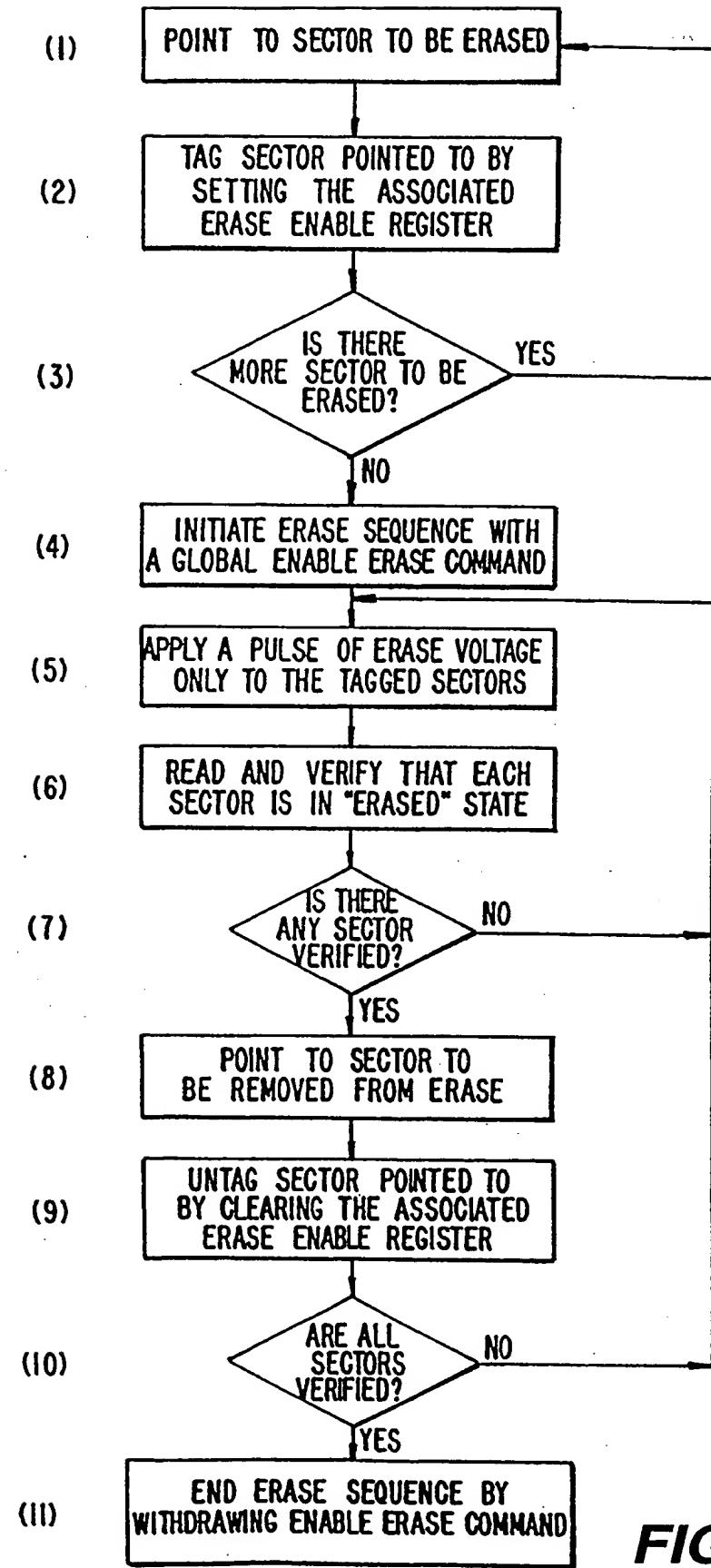


FIG._4



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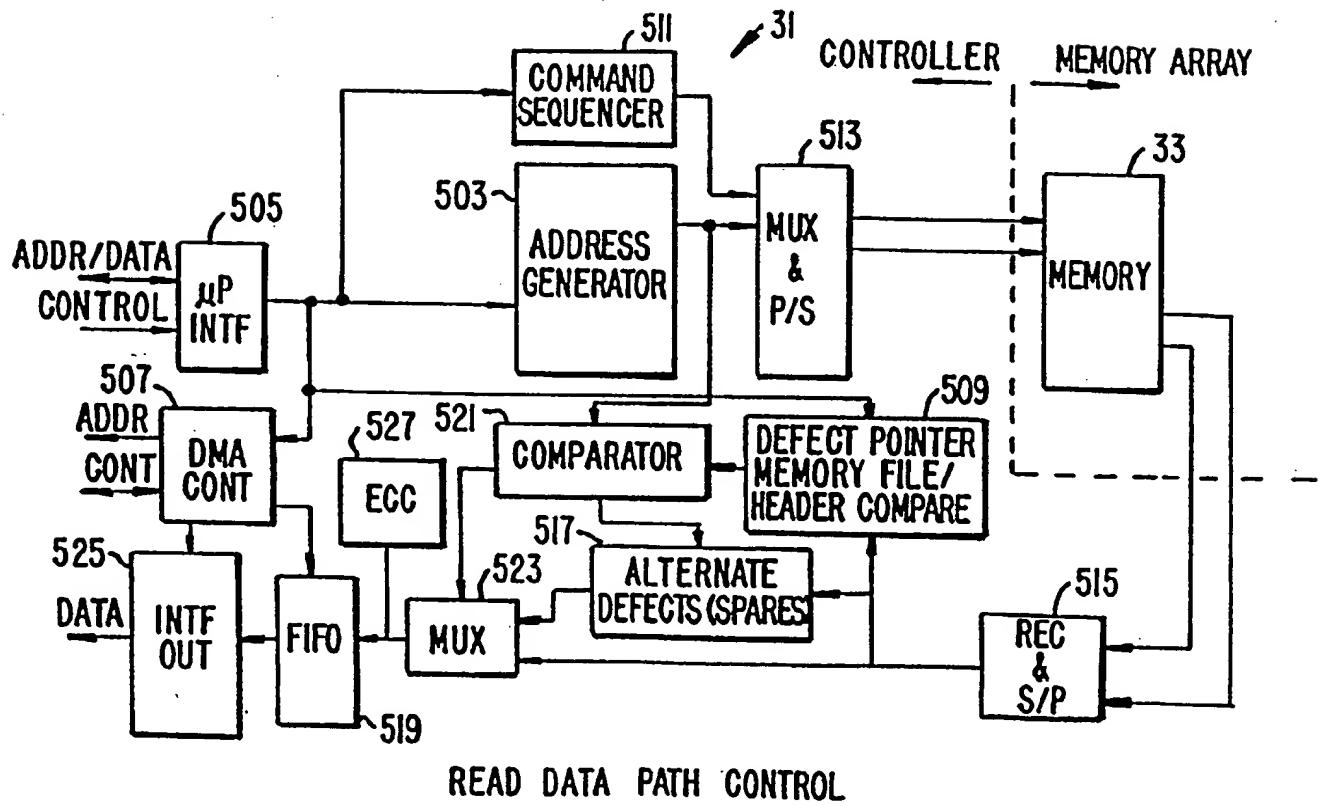
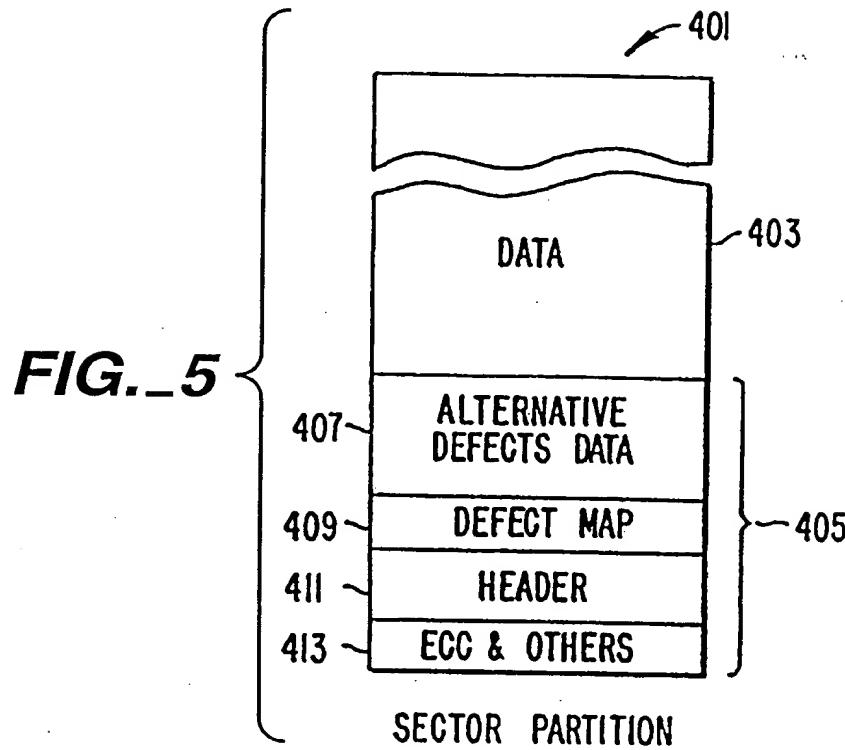
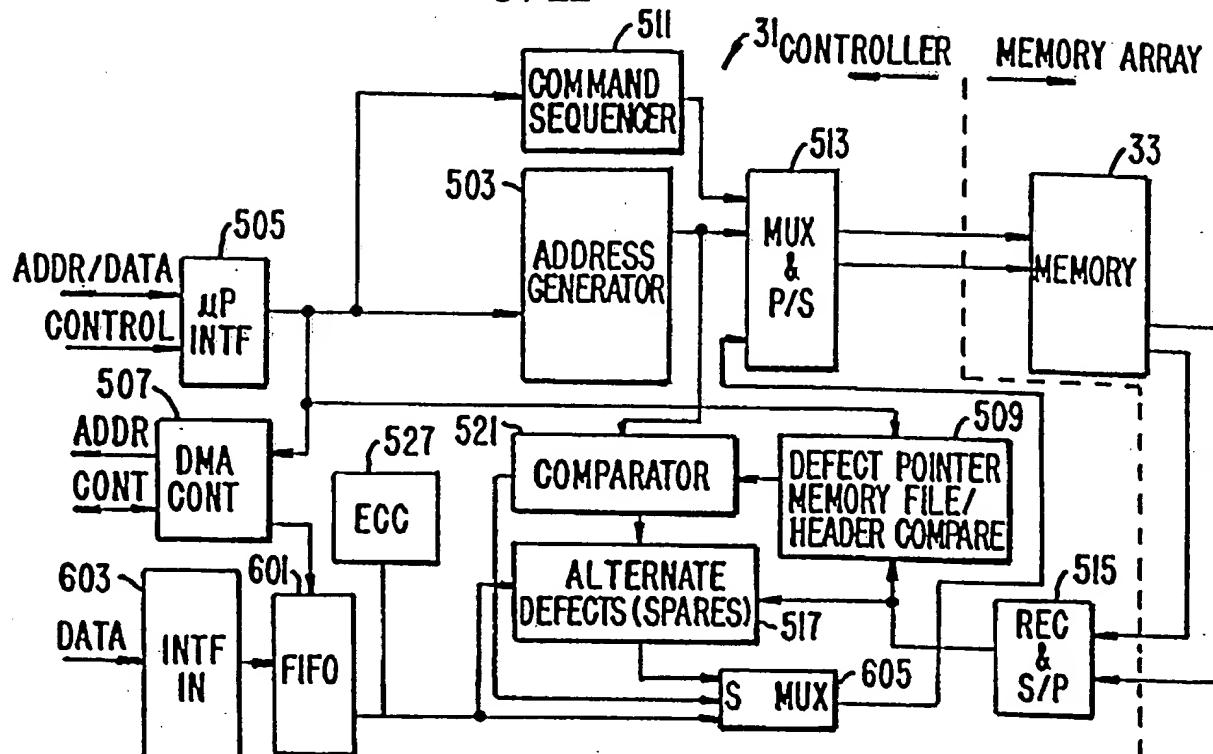


FIG. 6



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WRITE DATA PATH CONTROL

FIG. 7

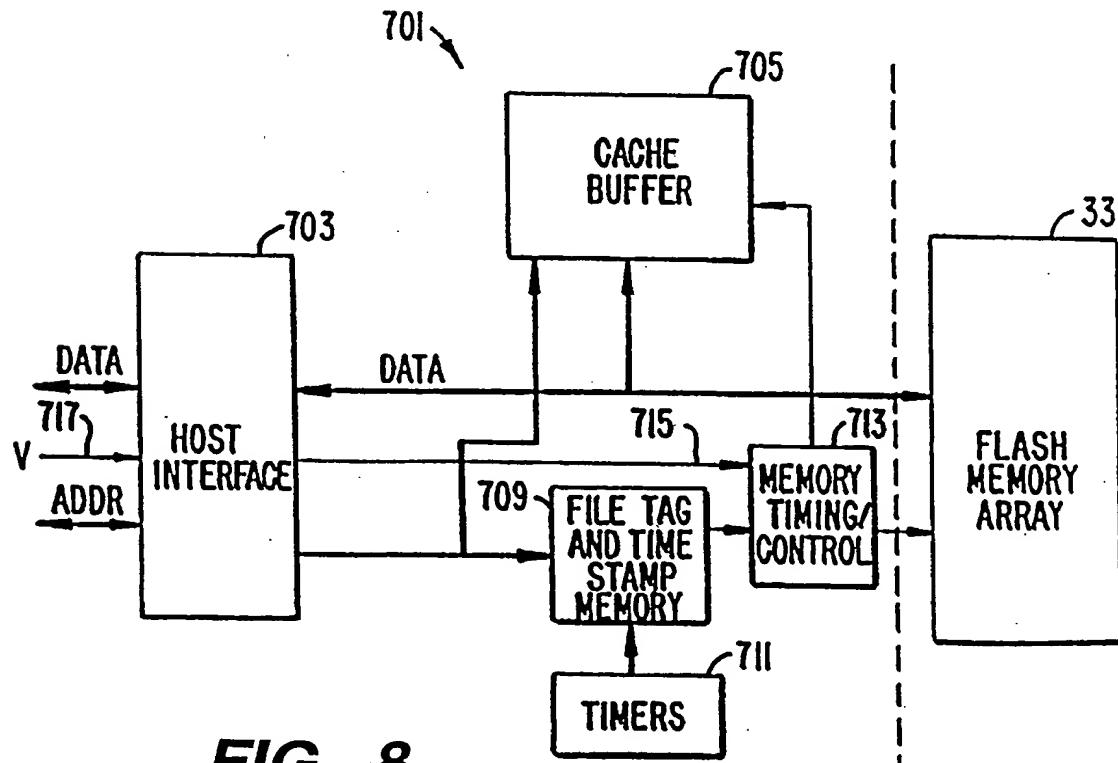


FIG. 8



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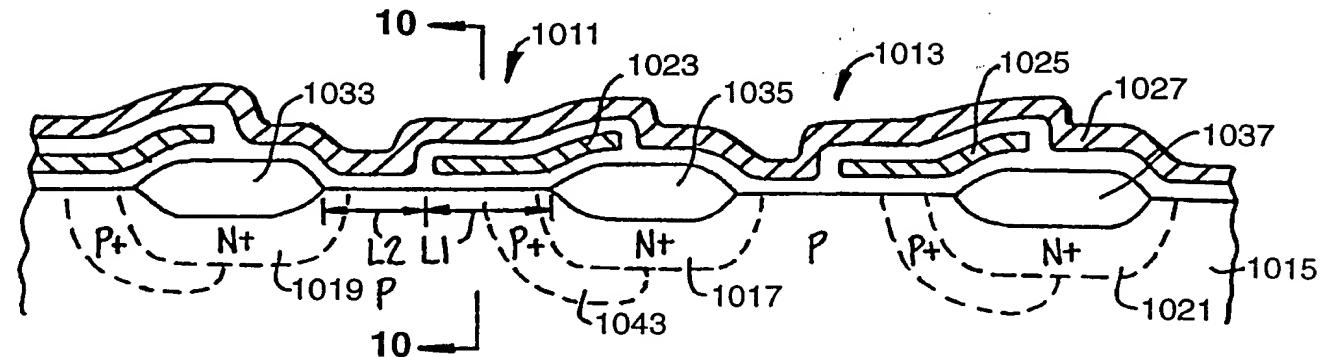


FIG. 9

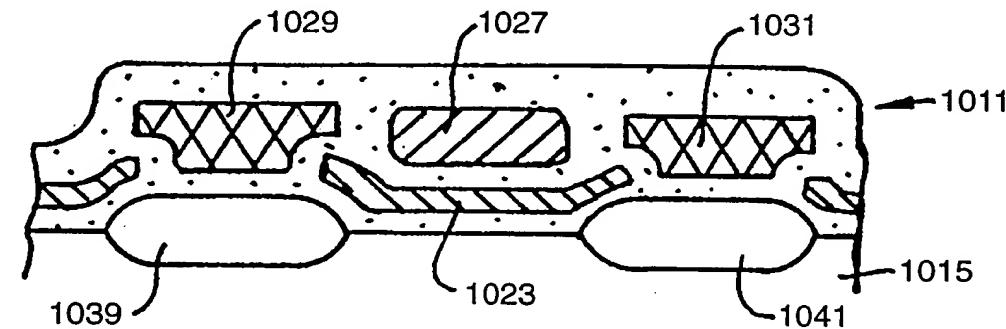


FIG. 10

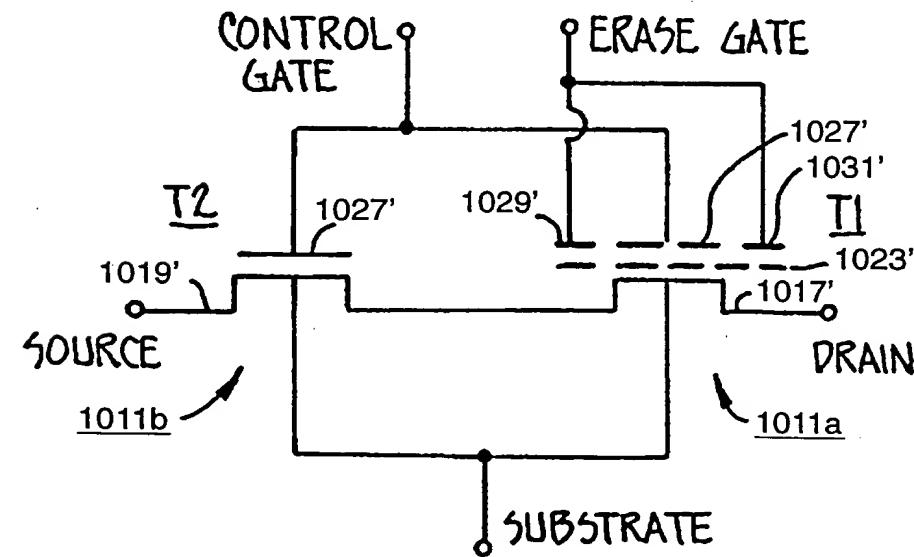


FIG. 11

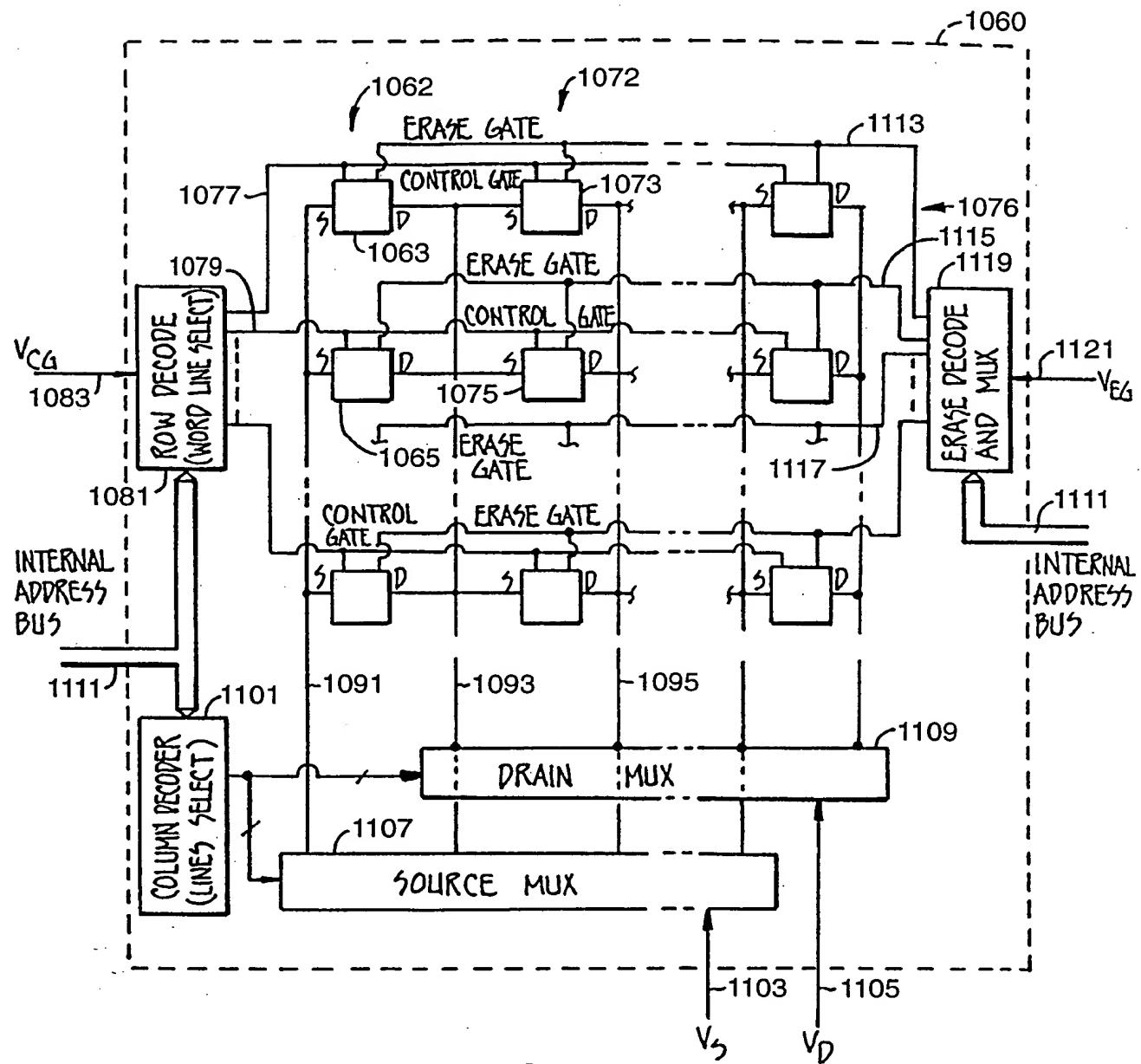


FIG. 12

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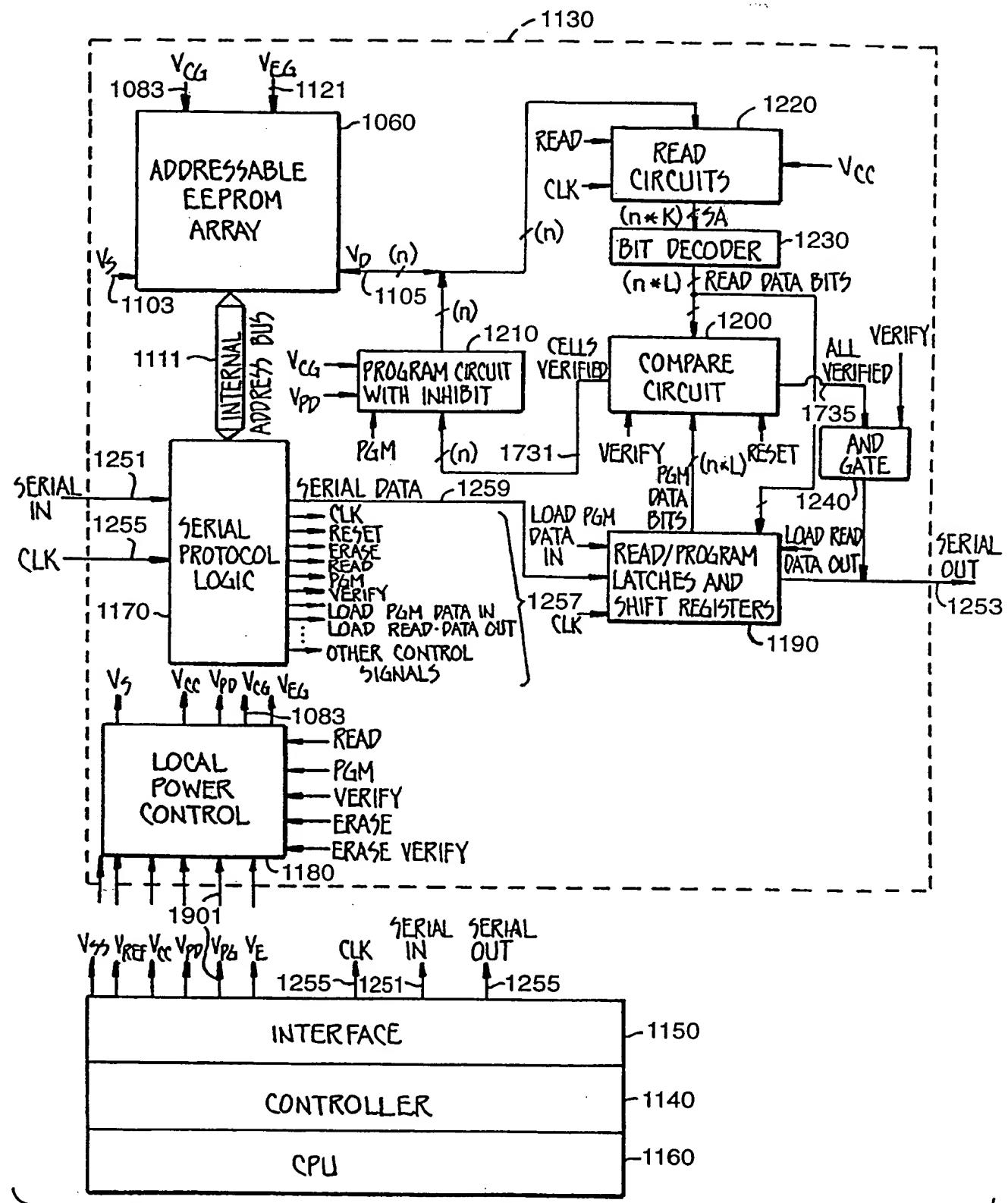


FIG. 13

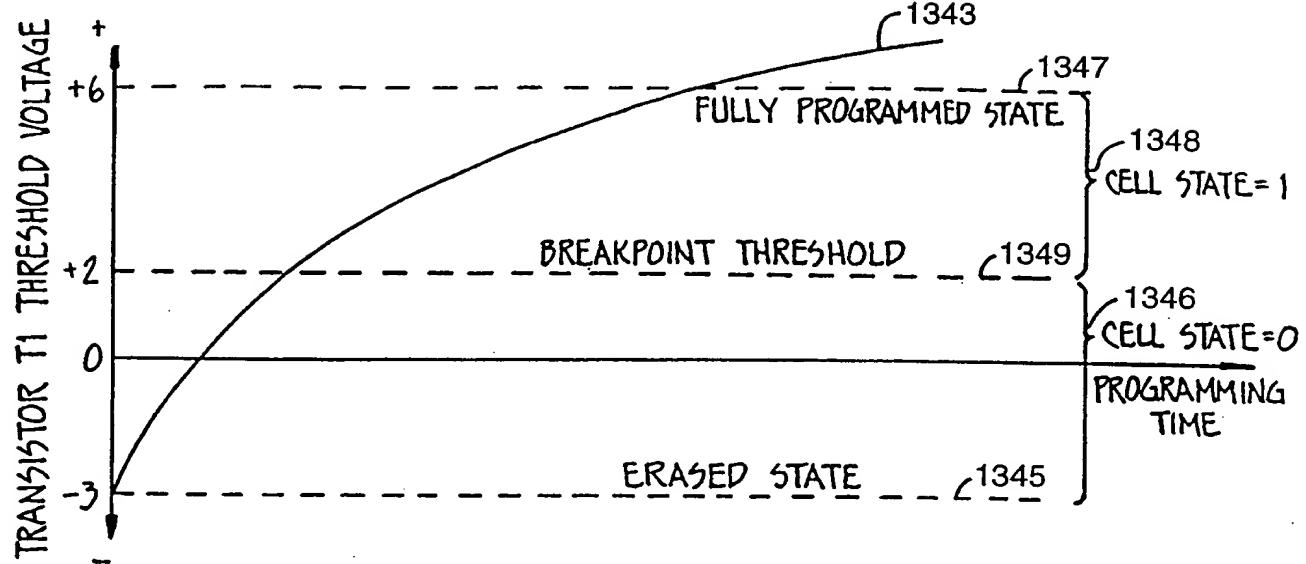


FIG. 14

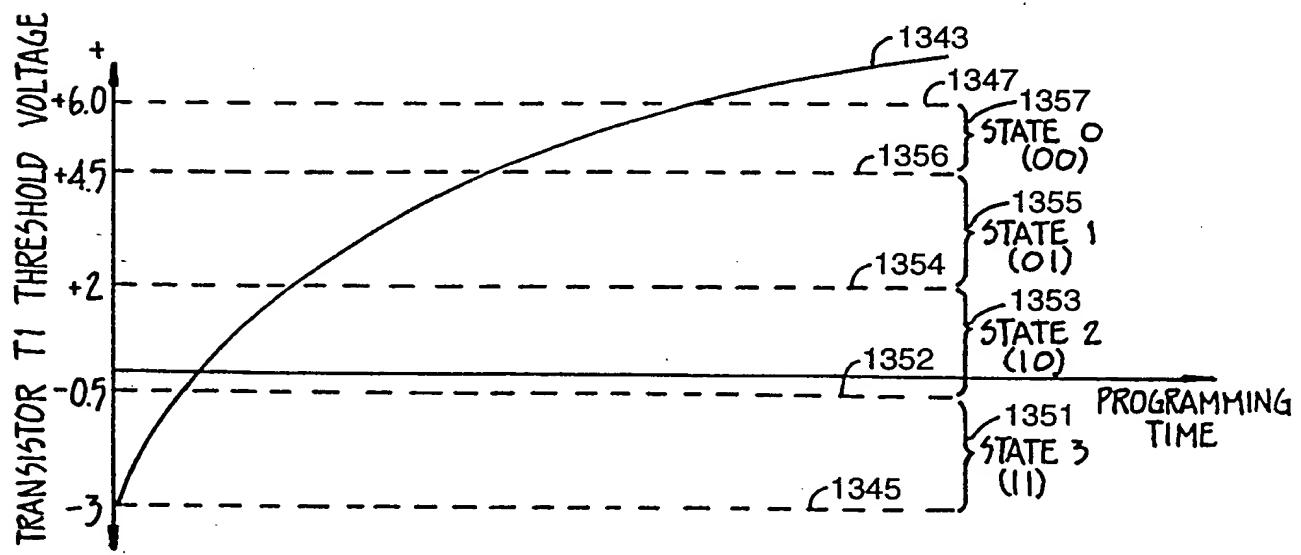


FIG. 15A

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Appn. No.: 09/759,119 Docket No.: SNDK.A06USS
Title: Flash EEPROM System
Inventors: Harari et al.
Filing Date: 1/11/01 Atty. Tel: (415) 318-1160 Sheet 10 of 22

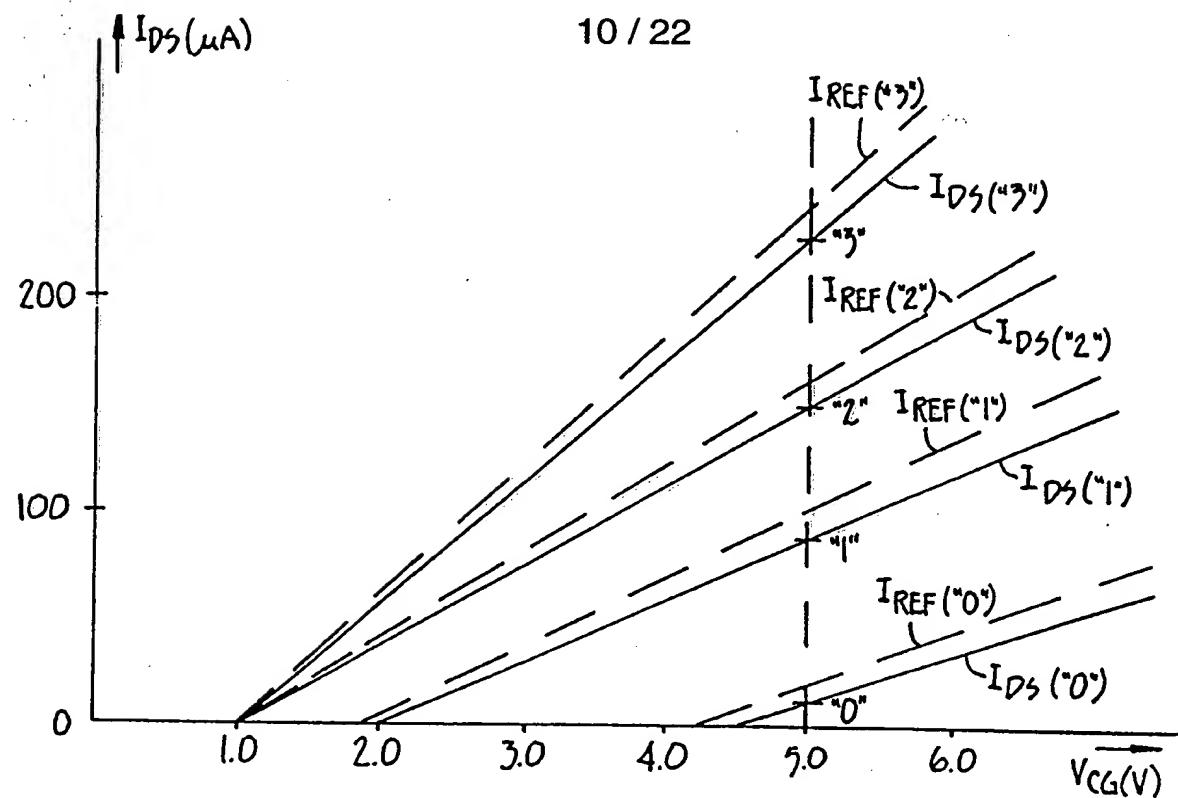


FIG._ 15B

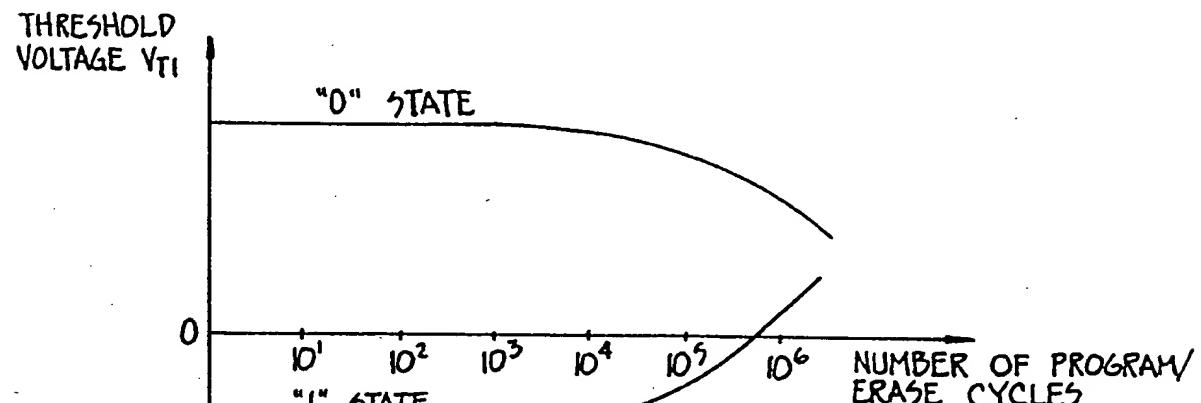


FIG._ 16A

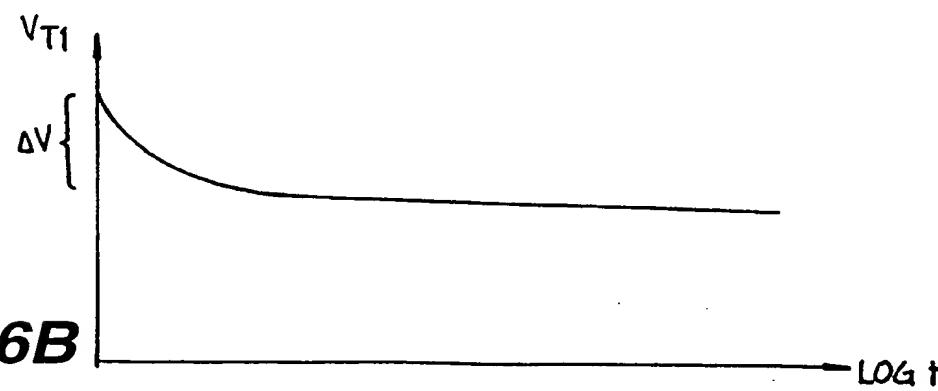


FIG._ 16B

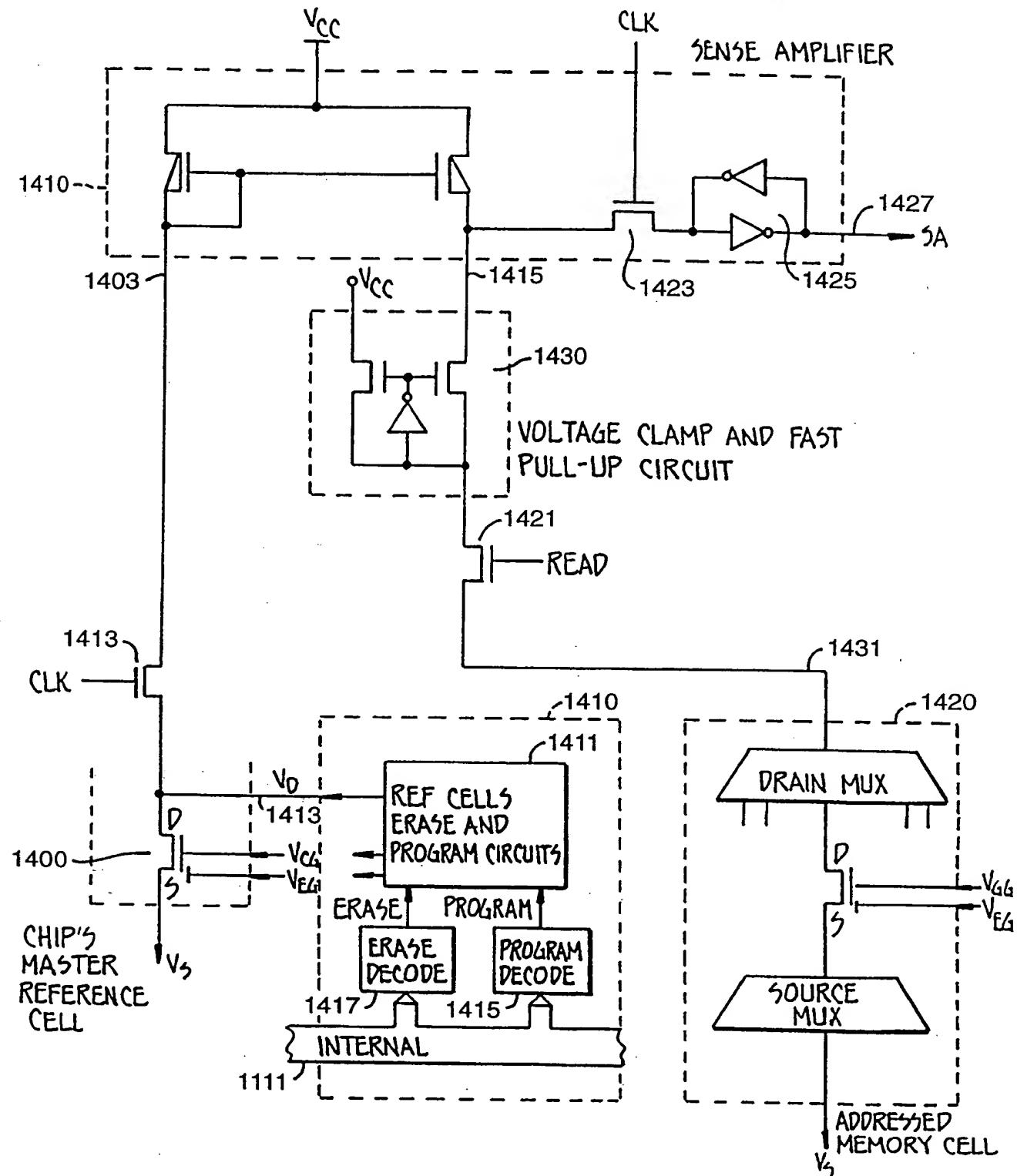


FIG.-17A



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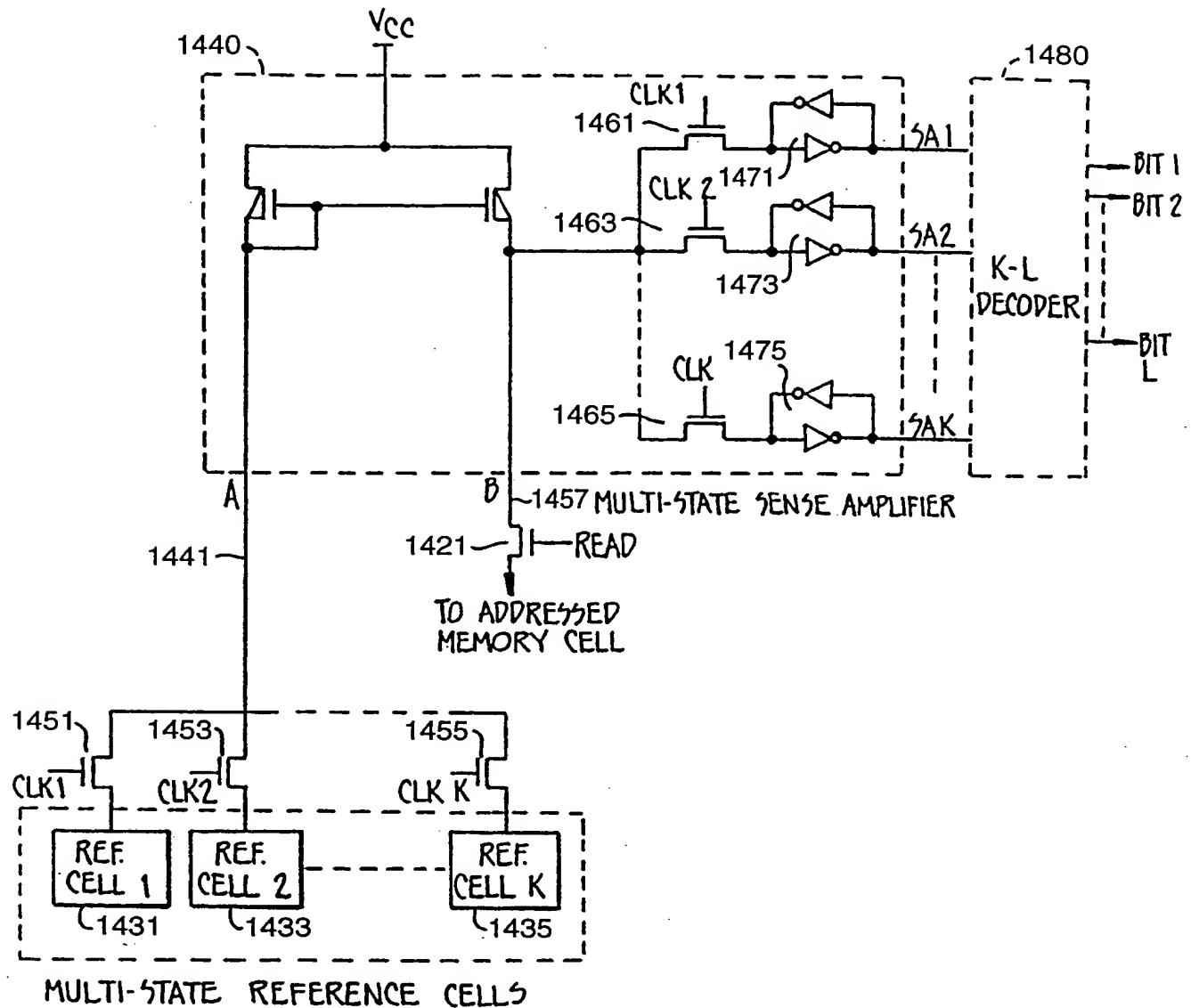


FIG._ 17B



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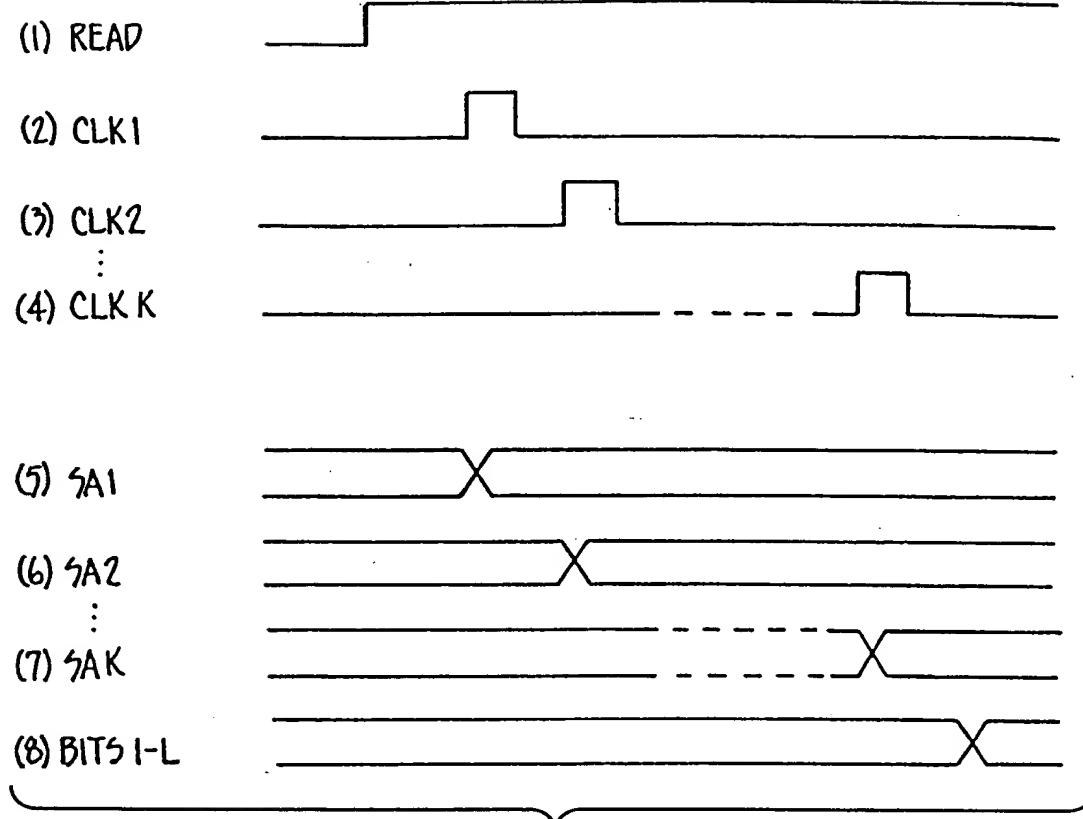


FIG._ 17C

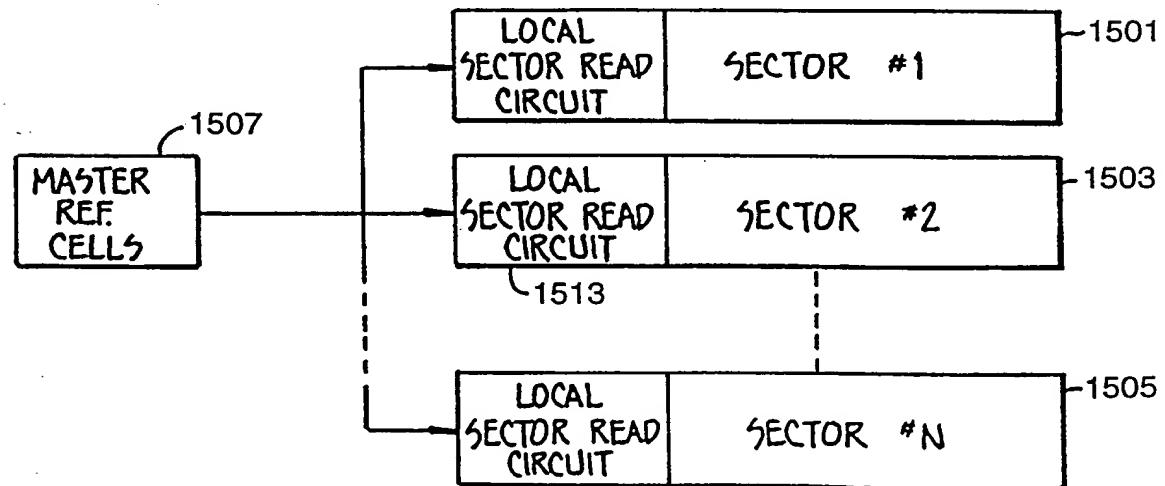


FIG._ 18

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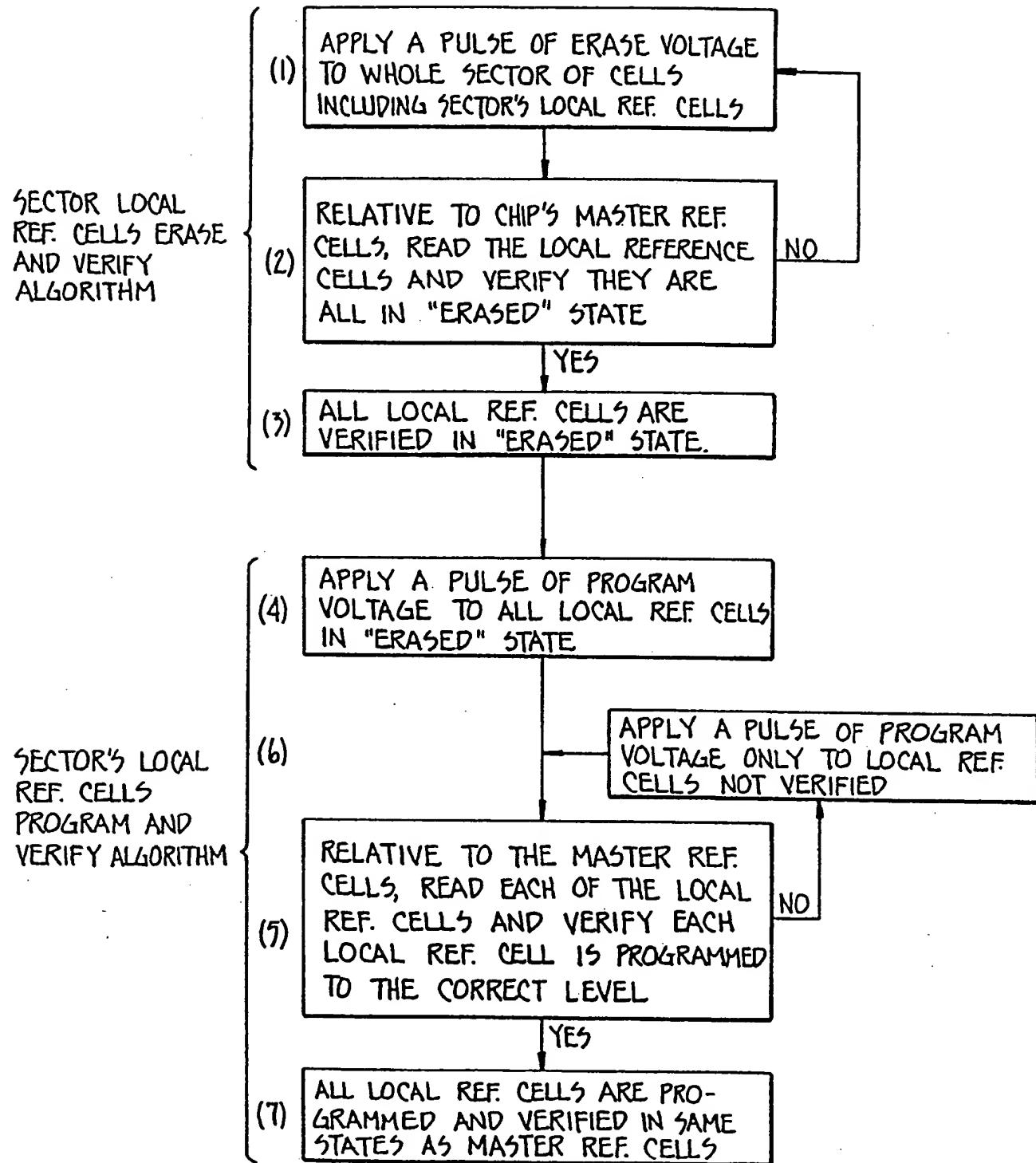


FIG. 19



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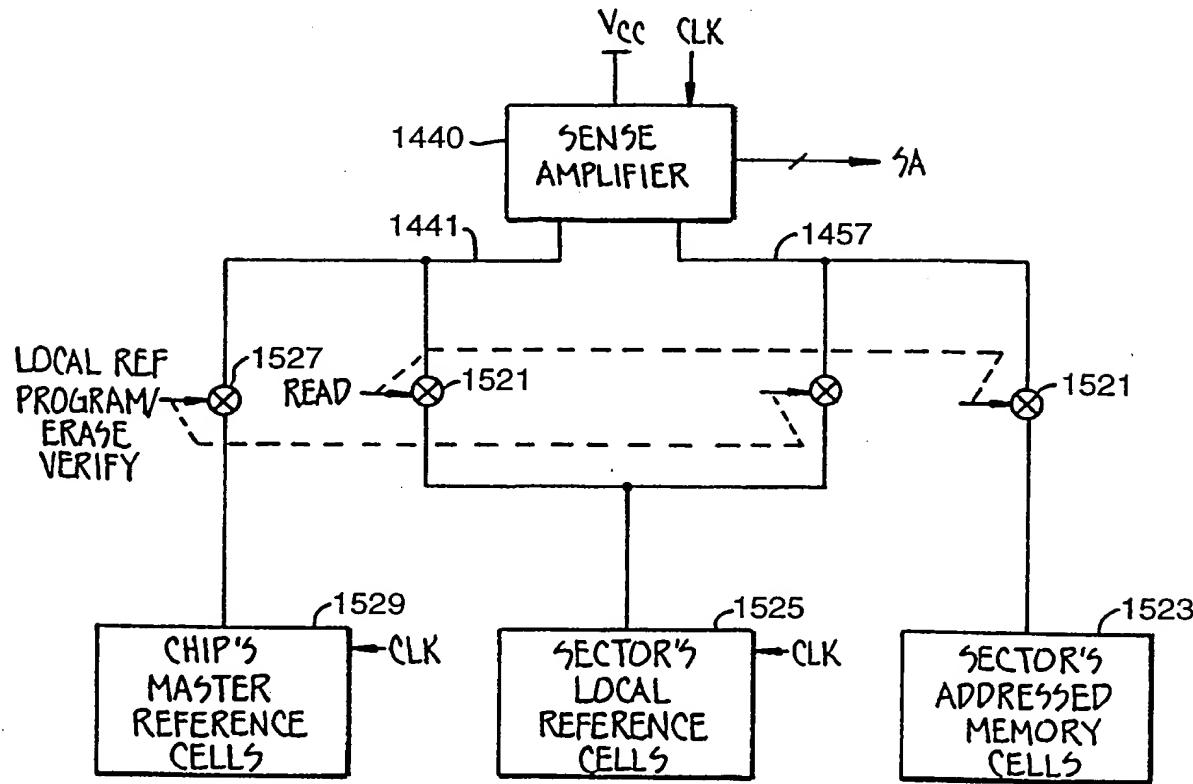


FIG._20A

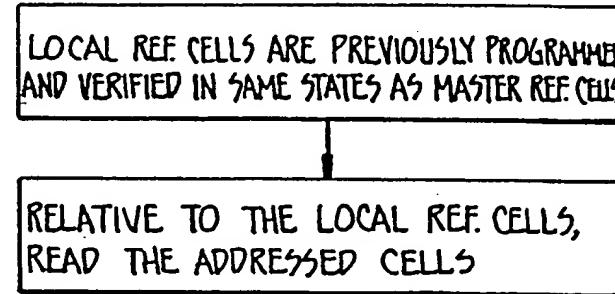
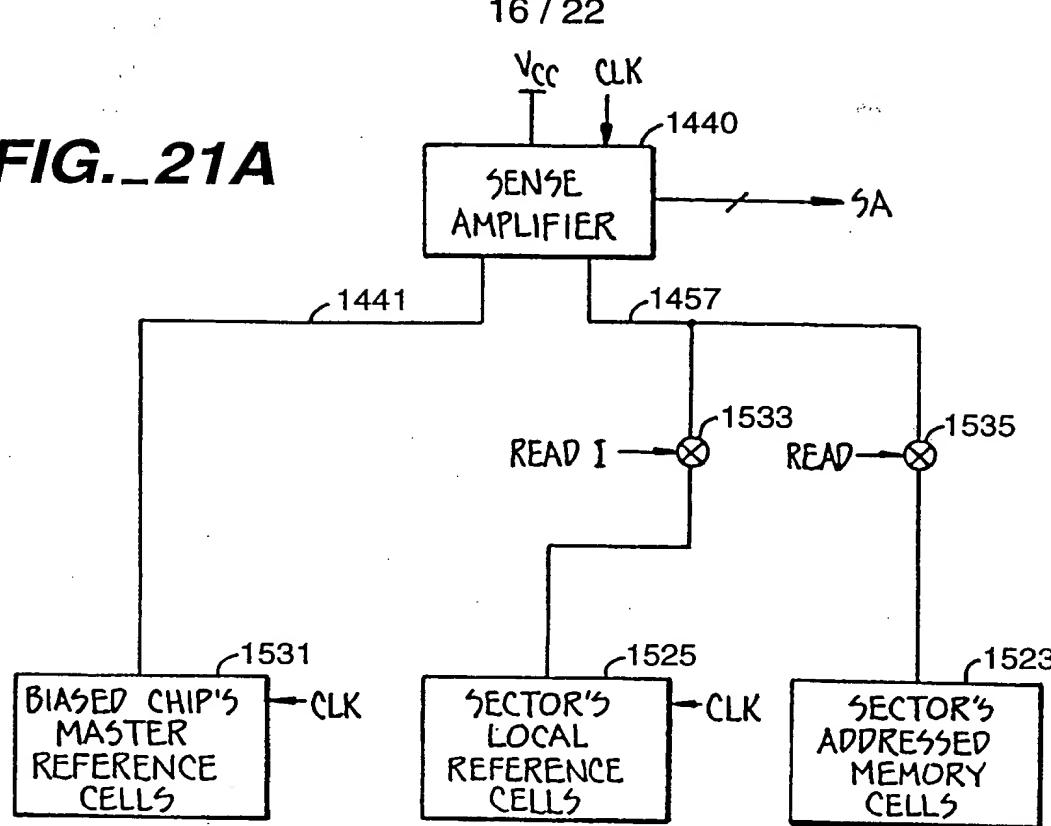


FIG._20B



FIG._21A



- (1) LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS
- (2) RELATIVE TO THE LOCAL REFERENCE CELLS READ THE MASTER REF. CELLS
- (3) DETERMINE THE DIFFERENCES, IF ANY AND BIAS THE MASTER REF CELLS' CURRENTS SUCH THAT THE SAME READING IS OBTAINED RELATIVE TO THE BIASED MASTER REF. CELLS AS RELATIVE TO THE LOCAL REF. CELLS
- (4) RELATIVE TO THE BIASED MASTER REF. CELLS, READ THE ADDRESSED CELLS

FIG._21D



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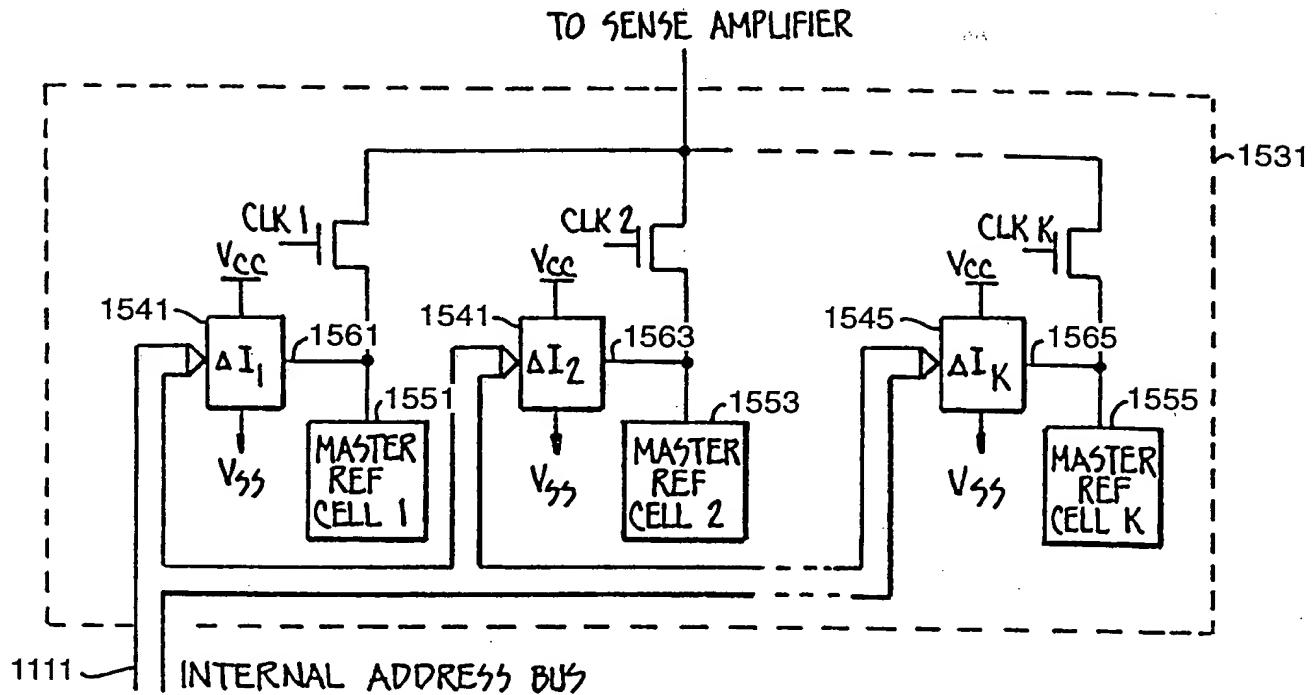


FIG. 21B

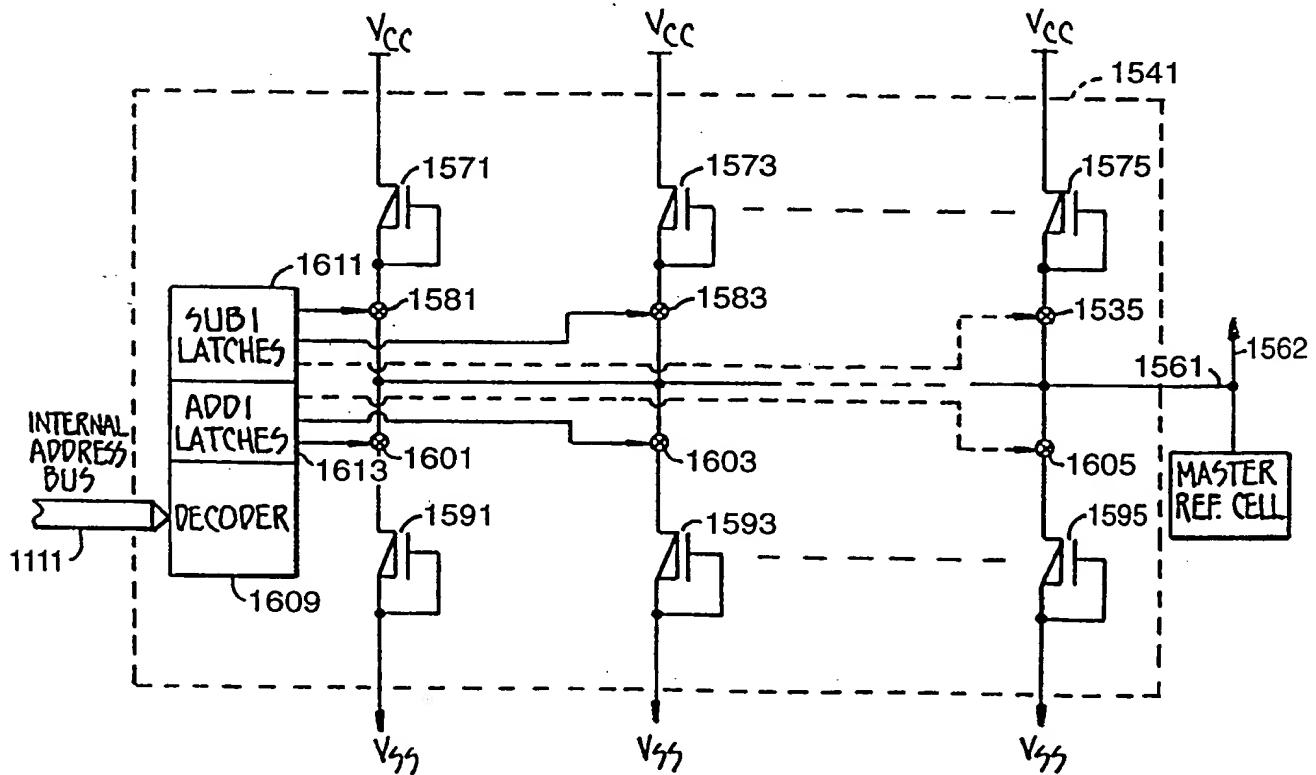
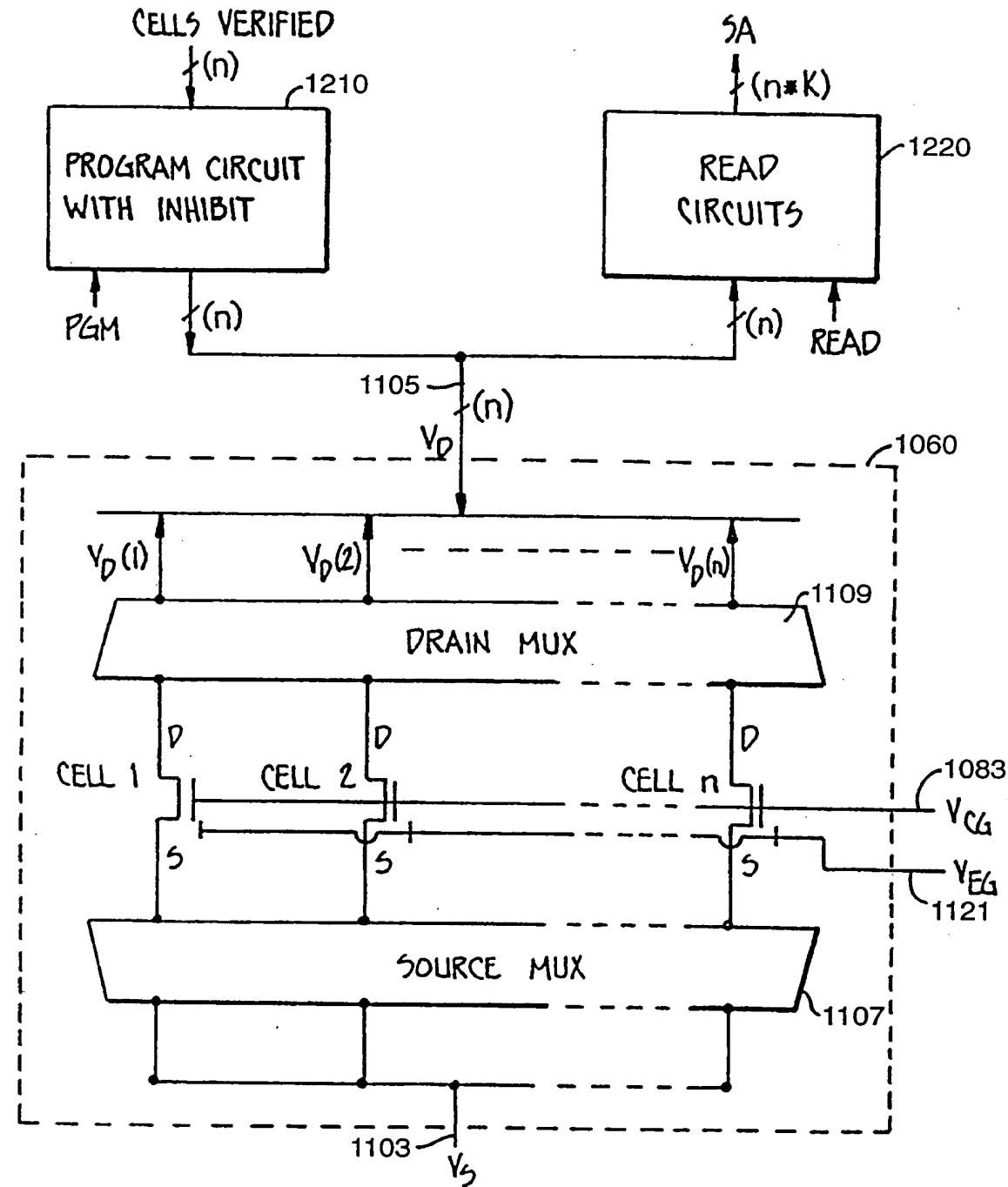


FIG. 21C

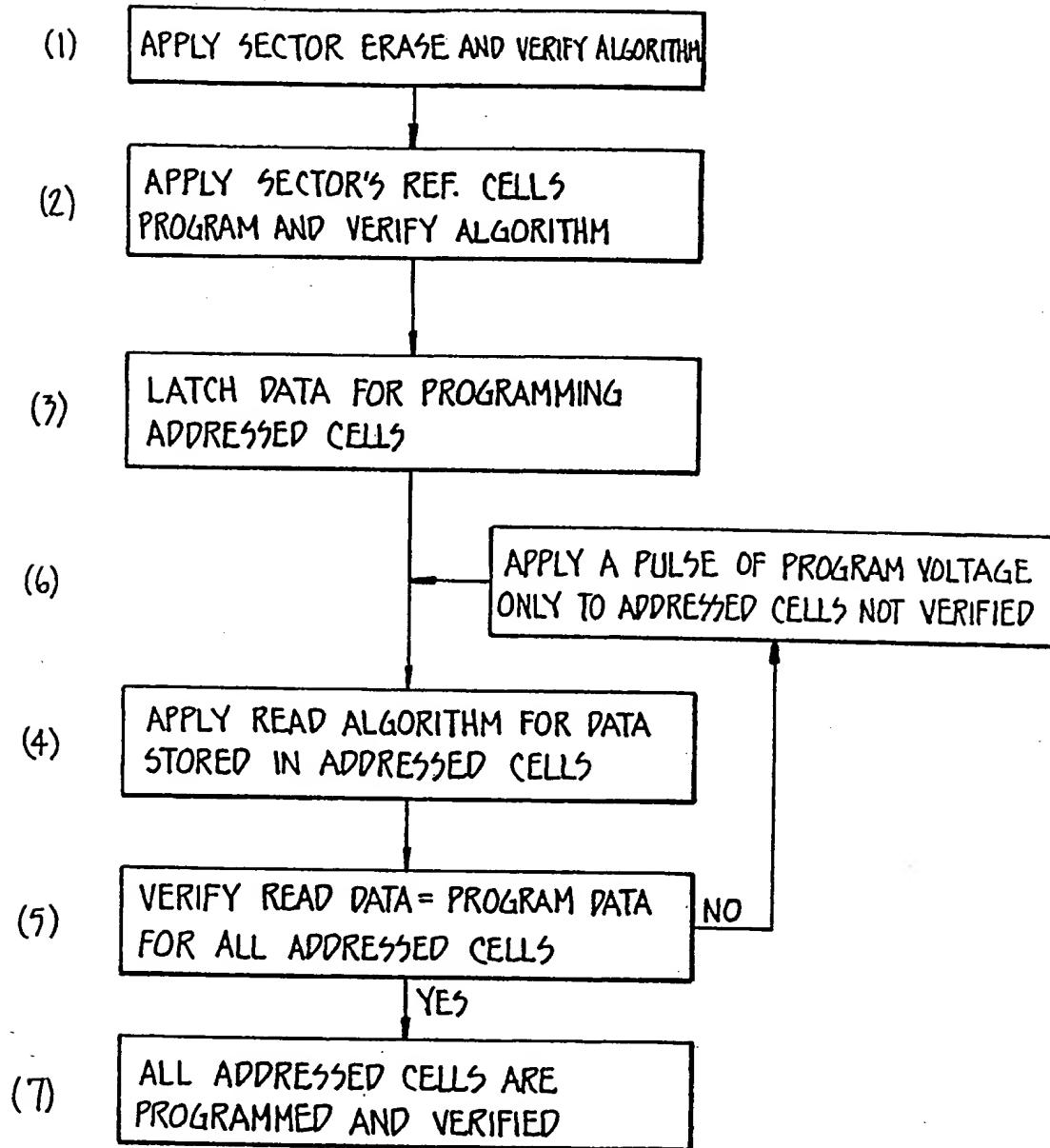


READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG._22



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PROGRAM ALGORITHM

FIG._23



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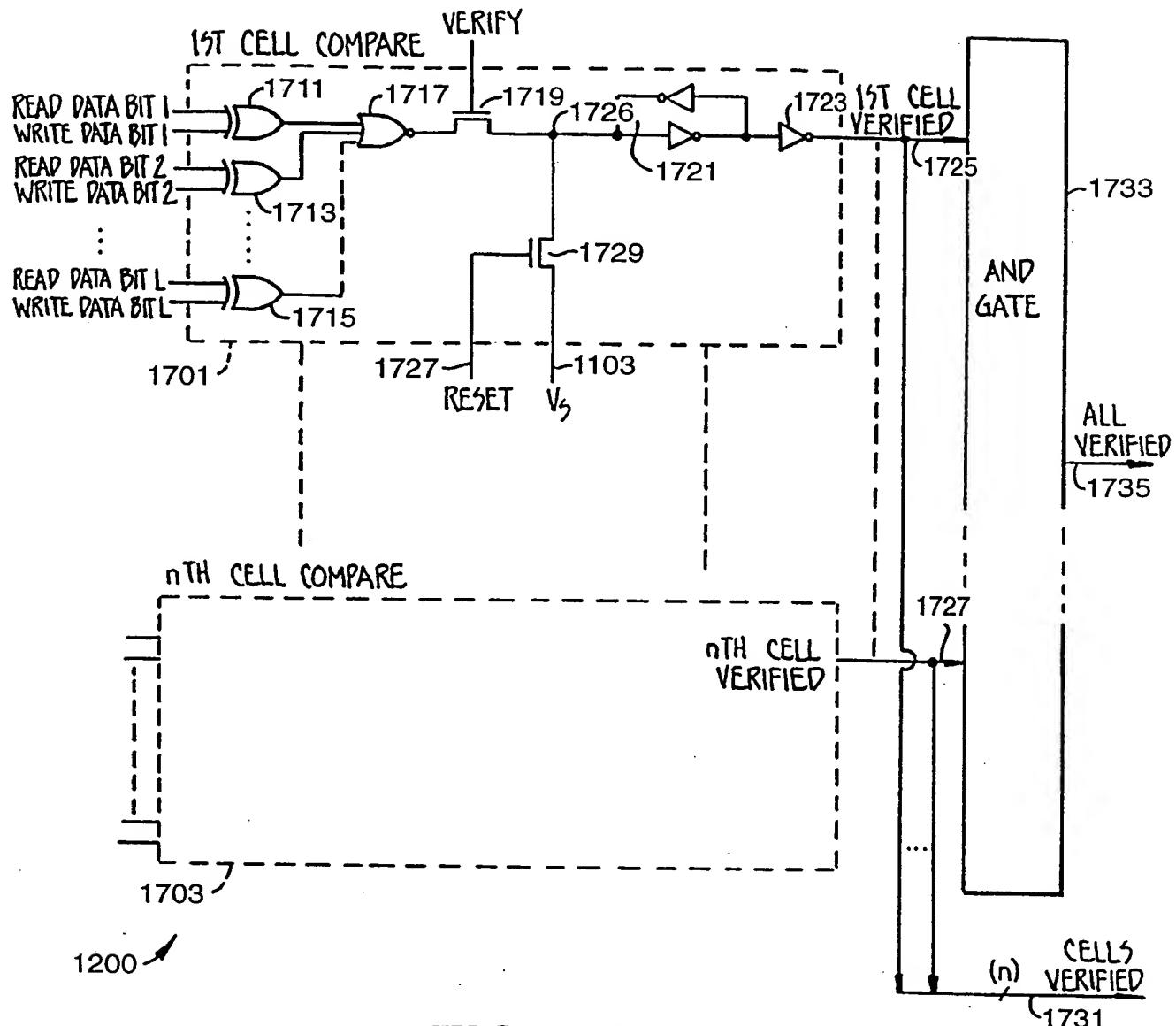


FIG.-24



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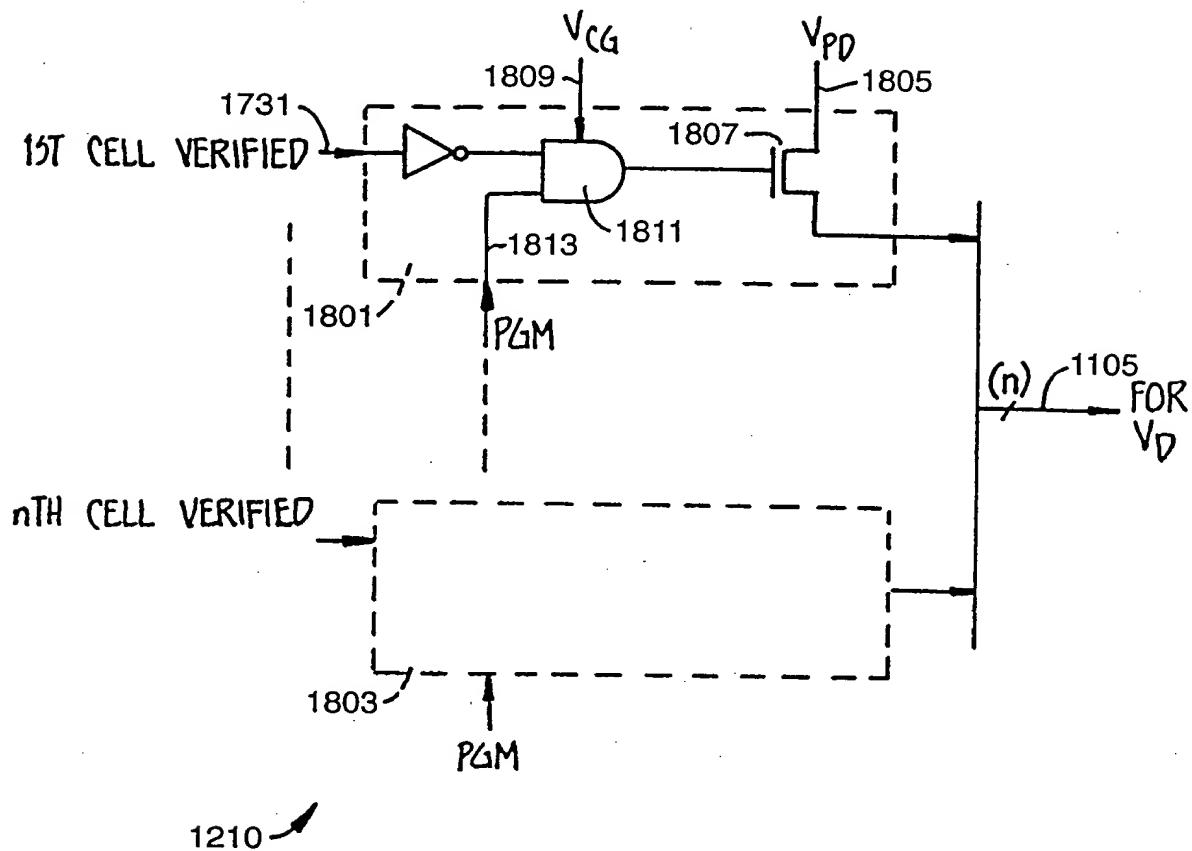


FIG. 25



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	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

TABLE 1

FIG._26

(TYPICAL VALUES)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC} + 5V$	V_{CC}	$V_{CC} - 5V$
V_{CC}	5V	5V	5V	5V	5V
V_{PD}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
UNSELECTED CONTROL GATE	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
UNSELECTED BIT LINE	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

$$V_{SS} = 0V, \quad V_{REF} = 1.5V, \quad SV = 0.5V - 1V$$

TABLE 2

FIG._27